REMARKS

Claims 1-8 have been examined and are all the claims pending in the application.

Claim Rejections - 35 U.S.C. § 103(a)

The Examiner has rejected claims 1-8 under 35 U.S.C. § 103(a) as allegedly being unpatentable over U.S. Patent No. 7,000,140 to Okubo et al. (hereinafter "Okubo") in view of U.S. Patent No. 4,434,696 to Conviser (hereinafter "Conviser") and further in view of U.S. Patent No. 6,346,833 to Kuroki (hereinafter "Kuroki"). Applicants submit that the claims are patentable and respectfully traverse the rejection.

For example, claim 1 recites a frequency multiplication circuit which multiplies a frequency of an input system clock, and a second frequency division circuit which divides the frequency of the signal output from the frequency multiplication circuit. A clock control means changes a frequency multiplication ratio of the frequency multiplication circuit to 1/N and changes a frequency division ratio of the second frequency division circuit to 1/N.

Okubo is directed to a data processor which includes a CPU 2 which can execute an instruction. A clock pulse generator 3 enables frequency multiplication and frequency division operation to a clock signal and outputs synchronizing clock signals CLK1, CLK2. The clock pulse generator 3 includes a PLL circuit 41 for multiplying a source clock signal 13, and frequency dividers 43, 44 which frequency divide the output of the PLL circuit 41 and output clock signals CLK1, CLK2 via selectors 45, 46 and output circuits 47, 48. Clock signal CLK1 is supplied to a built-in peripheral circuit 7, and clock signal CLK2 is supplied to the CPU 2. The

supply of the clock signals CLK1, CLK2 is suppressed or enabled based on a mode of operation of the data processor.

The Examiner seemingly contends that Okubo's PLL circuit 41 corresponds to the claimed frequency multiplication circuit and that Okubo's frequency divider 43, which supplies clock signal CLK1, corresponds to the claimed second frequency division circuit. However, referring to column 2, lines 11-28 of Okubo, the frequency multiplication and frequency division operation in the clock pulse generator 3 are *enabled* or *suspended*, and the clock signals CLK1 CLK2 are *supplied* or *stopped* depending on the mode of operation. Okubo further discloses that control signal 33 controls the *permission* and *prohibition* of the operation that outputs the clock signals CLK1 and CLK2, and that control signal 34 controls the *permission* and *prohibition* of the frequency multiplication and division operation (col. 6, lines 9-18). Thus, Okubo does not teach or suggest *changing* a frequency multiplication ratio of the alleged frequency multiplication circuit 41 to 1/N and *changing* a frequency division ratio of the alleged second frequency division circuit 44 to 1/N, as required by claim 1. Conversely, Okubo suggests that the ratios of the PLL circuit 41 and divider 43 are fixed, and that operation of these elements are turned on and off depending on a mode of operation.

On page 3 of the Office Action, the Examiner admits that Okubo does not teach or suggest the capability of showing the multiplication ratio of the PLL circuit 44 as 1/N and cites Conviser to supply this deficiency.

Conviser is directed to an instrument for comparing equal temperament and just intonation including a master-oscillator which supplies a primary reference frequency to a modulo-N counter. The modulo-N counter is used as a frequency divider whose divided frequency serves as the input signal to a phase-locked loop (PLL) having an output frequency controlled by a second modulo-M counter, which operates as a multiplier. Thus, a ratio of M/N is established for the two outputs.

The Examiner asserts that the ratio provided by Conviser's Modulo-M counter corresponds to the claimed 1/N frequency ratio. However, Conviser merely discloses that the modulo-M counter multiplies the frequency input to the PLL from the modulo-N counter, which divides the input frequency by N to provide the ratio M/N (col. 5, lines 34-47). Conviser does not teach or suggest a frequency multiplication ratio of 1/N for the alleged frequency multiplication circuit (modulo-N counter) *and* a frequency division ratio of 1/N for the alleged second frequency division circuit (modulo-M counter), as required by claim 1. At best, Conviser may suggest a multiplication ratio of 1/N and a division ratio of 1/M to result in the expression (1/N) / (1/M) which provides Conviser's disclosed ratio of M/N. However, referring to Table 1, Conviser does not teach or suggest a case in which M is equal to N. Thus, Conviser does not teach or suggest the claimed ratios.

Furthermore, Conviser discloses that a series of M/N stages, to make a total of 12 outputs, will provide all of the required frequencies and that the numerical values for M and N shown in Table 1 give *precise* ratios for a scalar representation of intervals (col. 4, line 65 to col. 5, line 4). Clearly, the values for M and N are *predetermined and fixed.* Thus, Conviser does not

supply the deficiency of Okubo discussed above because Conviser does not teach or suggest *changing* a frequency multiplication ratio of the alleged frequency multiplication circuit 41 to 1/N and *changing* a frequency division ratio of the alleged second frequency division circuit 44 to 1/N, as required by claim 1.

On page 3 of the Office Action, the Examiner acknowledges that neither Okubo nor Conviser teach that N is a positive integer and relies on Kuroki to supply this deficiency. Kuroki discloses a frequency multiplier circuit 10 which includes a variable frequency divider 14 which is provided with variable frequency division data n (n is a positive number) from the outside. However, Kuroki does not supply the aforementioned deficiencies of Okubo and Conviser. Specifically, Kuroki does not teach or suggest a frequency multiplication ratio of 1/N for the alleged frequency multiplication circuit (modulo-N counter) *and* a frequency division ratio of 1/N for the alleged second frequency division circuit (modulo-M counter), as required by claim 1.

Moreover, Kuroki does not teach or suggest *changing* a frequency multiplication ratio of the alleged frequency multiplication circuit 41 to 1/N and *changing* a frequency division ratio of the alleged second frequency division circuit 44 to 1/N, as required by claim 1. Although Kuroki's frequency multiplier circuit 10 is supplied with a *variable* frequency divider 10, Applicants submit that one of ordinary skill would not have been motivated to combine this feature with the teachings of Conviser to reach the above recited limitation. The Examiner asserts that one of ordinary skill in the art would have modified the invention of Okubo with the teaching of Conviser and Kuroki to provide all of the required frequencies of the equally-

tempered scale based on the 12^{th} root of 2 and exponents thereof for as many octaves as desired. However, as discussed above, Conviser discloses that the numerical values for M and N shown in Table 1 give *precise* ratios for a scalar representation of intervals (col. 4, line 65 to col. 5, line 4). Conviser's teachings of *fixed* values for M and N clearly teaches away from Kuroki's *variable* frequency divider 10.

For all of the foregoing reasons, Applicants submit that the combination of Okubo, Conviser, and Kuroki does not render claim 1 unpatentable and respectfully request withdrawal of the rejection.

Independent claims 3, 5, and 7 recite features which are similar to those discussed above in conjunction with claim 1. Thus, Applicants submit that claims 3, 5, and 7 are patentable at least for reasons analogous to those discussed above regarding claim 1. Applicants also submit that claims 2, 4, 6, and 8, being dependent on claims 1, 3, 5, and 7, respectively, are patentable at least by virtue of their dependency. Thus, withdrawal of the rejection is respectfully requested.

Conclusion

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,

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